Journal of Materials Science: Materials in Electronics
https://doi.org/10.1007/s10854-018-00650-w

Design impact on the performance of Ge PIN photodetectors

Xuewei Zhao[1,2] · M. Moeen[5] · M. S. Toprak[5] · Guilei Wang[2,3] · Jun Luo[2,3] · Xingxing Ke[2,3] · Zhihua Li[2,3] · Daoqun Liu[2,3] · Wenwu Wang[2,3] · Chao Zhao[2,3] · Henry H. Radamson[2,3,4]

Received: 28 November 2018 / Accepted: 26 December 2018

Abstract
This article presents the impact of epitaxial quality, contact resistance and profile of Ge PIN photodetectors (PDs) on dark current and responsivity. The PD structures were processed with either selectively grown Ge with integrated waveguides on SOI wafer or globally grown Ge on the entire wafer. The contact resistance was lowered by introducing NiGe layer prior to the metallization. The n-type doped Ge PIN structure was formed by ion implantation and the contact resistivity was estimated to 2.6×10^{-4} Ω cm^2. This value is rather high and it is believed to be due to fomation of defects during implantation. The results show a minor difference in dark currents for selectively and globally grown PDs but in both types, it depends on detector area and the epitaxial quality of Ge. For example, the threading dislocation density (TDD) in non-selectively grown PDs with thickness of 1 µm was estimated to be 10^6 cm^{-2} yielding relatively low dark currents while it dramatically changes for PDs with thinner Ge layers where TDD increases to 10^8 cm^{-2} and the dark current levels increase almost by 1.5 magnitude. Surprisingly, for selectively grown PDs with Ge thickness of 500 nm, TDD was still low resulting in low dark currents. The dark current densities at − 1 V bias of non-selectively and selectively grown PDs with optimized profile were measured to be 5 mA/cm^2 and 47 mA/cm^2, respectively, while the responsivity of these detectors were 0.17 A/W and 0.46 A/W at λ ~ 1.55 µm, respectively. Excellent performance for selectively grown PD shows an appropriate choice for detection of 1.55 µm wavelength.

1 Introduction

Silicon-based photonics has been developing rapidly with the increasing demand for information capacity and transmission rate. Because of its compatibility with CMOS technology, high photon transmission rate and strong anti-interference, silicon photonics has brought great hopes for the new direction of Moore's Law. Therefore, silicon photonics technology has been a focus of attention in recent years.

Ge has high absorption coefficient and high carrier mobility in the near-infrared region (NIR), making it widely used in silicon-based photonics integration. In order to achieve high-quality Ge or GeSi PDs with low dark current and high responsivity, a series of research activities have been presented in this field employing different methods [1–12].

One of the early reports of SiGe based PIN detectors was released by Luryi et al. [1] by using Molecular beam epitaxy (MBE) to grow graded Ge_xSi_{1-x} as a buffer layer followed by the growth of Ge layer. The quantum efficiency of the detector prepared by this design was 41% at $T=300$ K. Shortly afterwards, Currie et al. [2, 3] used the same design of detector but chemo-mechanical polishing (CMP) was applied in graded SiGe layers to control threading dislocation densities (TDD) in Ge layer. In this method, TDD in the Ge layer was reduced to 2.1×10^6 cm^{-2} and the dark current density of detectors was measured to 0.15 mA/cm^2. Chemical Vapor Deposition (CVD) technique was used by Huang et al. who

✉ Jun Luo
luojun@ime.ac.cn

✉ Zhihua Li
lizhihua@ime.ac.cn

✉ Henry H. Radamson
rad@ime.ac.cn

1 University of Science and Technology of China, Hefei 230026, Anhui, People's Republic of China

2 Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China

3 University of Chinese Academy of Sciences, Beijing 100049, People's Republic of China

4 Department of Electronics Design, Mid Sweden University, Holmgatan 10, Sundsvall 851 70, Sweden

5 KTH Royal Institute of Technology, Stockholm, Sweden

Published online: 25 January 2019

reported Ge PDs by using two intermediate buffer layers of 1 µm [4]. The dark current was significantly improved to 1.07 µA at − 10 V and responsivity value of 0.57 A/W at 2 V reverse bias. Although the graded SiGe layer can achieve high relaxation of the epitaxial Ge layer, the SiGe layer has to be thick which is inconvenient for integrating on the Si-based circuit.

An innovative profile for Ge PD structure was presented by Colace et al. where Ge layer was grown directly on Si by using a two-step temperature growth (330 °C 50 nm + 500 °C 300 nm). This design of Ge detector showed responsivity of 0.12 A/W at 1300 nm and a leakage current density of 1 nA/cm^2 [5]. Dongwoo et al. also applied a two-step temperature growth (400 °C 100 nm + 500 °C 1.2 µm) and demonstrated responsivity of 0.47 A/W at 1.55 µm and the dark current density of 18.5 mA/cm^2 at − 1 V [6].

Using selective heteroepitaxy combined with the two-step growth has also been proposed. In such device, a responsivity of 0.64 A/W at 1.55 µm and a dark current density of 3.2 mA/cm^2 were achieved [7]. More improvements were carried out by Yin et al. when a PIN Ge detector was combined with a high performance waveguide. They integrated waveguide with selectively grown Ge detector on a SOI substrate. Such detector demonstrated responsivity of 0.89 A/W at the wavelength of 1.55 µm and the dark current of 169 nA at − 2 V [8]. Later, Chen et al. manufactured PIN PDs integrated with waveguide by adopting a 160 nm thin germanium layer to reduce the transmit time and they demonstrated high bandwidth of 67 GHz and the measured responsivity was 0.72 A/W at − 1 V [10].

Although, the various reports indicate the tremendous effort to improve the dark current of the Ge PDs, however until now, no extensive study has been devoted to promoting the better understanding of dark current mechanisms, responsivity and waveguide integration. Therefore, this study presents two designs for Ge PDs: selectively and non-selectively grown Ge PIN structures with and without waveguide integration where the focus was placed on the behavior of dark current and responsibilty.

2 Experimental details

In this work, four options have been considered in the design of the Ge PD as illustrated in Fig. 1. These options are listed as: growth method of Ge layer (SEG versus NSEG), variation of the intrinsic layer thickness in the PIN structure, and the profile of the starting Ge layer on Si wafer.

The choice of the growth technique is important since after the germanium layer is deposited onto the Si wafer, dry etch is applied to form mesas. This issue is of concern during the dry etching process when the Ge-layer sidewalls are exposed to plasma and may be damaged by ions. The other issue related to the choice of Ge growth technique is related to TDD: since in SEG the Ge crystal is grown inside an oxide opening and TDD may differ compared to the global growth on the entire wafer.

Another approach to deal with the defect density in PIN Ge layers is to tailor the starting layer. Two approaches can be tried: a graded SiGe or a direct Ge growth on the Si wafer.

All detectors in this study were manufactured on 8-inch (100) wafers. After a standard cleaning, a Ge layer with thickness of 400 nm was grown at low temperature (LT) of 400 °C. This layer has high TDD since it contains the initial nucleation Ge on Si. As an alternative to this LT-Ge layer a graded SiGe from Si to pure Ge layer has been also examined. After the growth of the initial layer, a PIN structure with high epitaxial quality was deposited at high temperature (HT) around 650 °C. At first, a highly B-doped layer of 300 nm is formed, followed by the growth of 0.3–1 µm intrinsic layer. Finally, a baking at 850 °C is performed to reduce the defect density. The n-type layer was formed by ion implantation with thickness of ~ 100 nm.

2.1 Process of PD with global growth design

Global or non-selective epitaxy growth (NSEG) refers to Ge-layer deposition on the entire wafer. The NSEG of Ge was performed using GeH_4 as Ge precursor. In PIN structures, after P-type and intrinsic layer were grown, the N-type

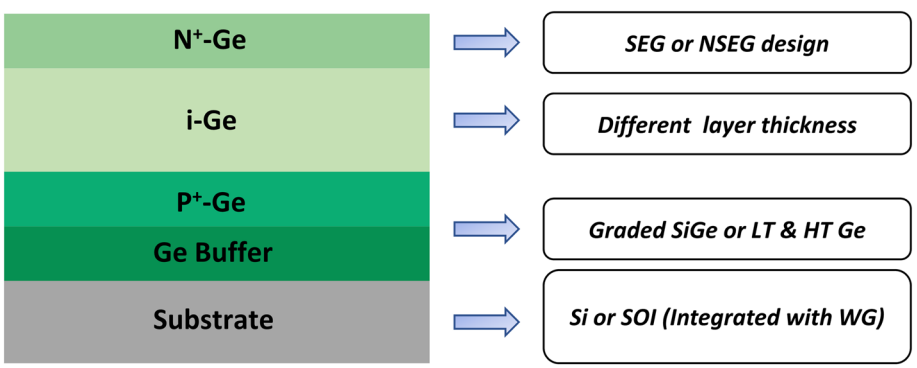


Fig. 1 Epitaxy methods and profile of Ge PIN detector

layer was formed by ion implantation with dose and energy of 2×10^{15} cm^{-2} and 5 keV, respectively. Afterwards, an annealing treatment at 600 °C in hydrogen for 60 s was performed. The process of detector patterning included three steps of photolithography and etching. Mesas with diameters varying from 10 to 100 µm were defined. A 300 nm-thick SiO_2 was deposited as a passivation layer and an anti-reflection film by Plasma Enhanced Chemical Vapor Deposition (PECVD). Then SiO_2 layer was selectively etched by a capacitive coupled plasma (CCP) etcher to form the contact electrode holes. A Ti/TiN/AlSi stack with thickness of 50 nm/12 nm/400 nm was deposited by Physical Vapor Deposition (PVD) and dry etching was performed to form metal electrodes as illustrated in Fig. 2a.

2.2 Process of PD with selective epitaxy growth design

The selective epitaxy growth (SEG) is a deposition inside a trench in the insulator (oxide or nitride layer). SEG of Ge layer was obtained using GeH_4 and HCl reactant gases. The PIN PDs in this design were integrated with Si waveguide. The PDs were processed on 8-inch P-type SOI wafers with 2 µm buried oxide layers and 220 nm Si top layers. A thin SiO_2 layer was formed on the SOI wafer by thermal oxidation prior to depositing the 150 nm-thick poly-Si. In order to enhance the optical coupling efficiency between the optical waveguide and the detector, a wedge-shaped structure with a thickness of 150 nm was etched in the Poly-Si layer [10]. Later, 70 nm of the top Si was etched to form a focus grating coupler.

The N-type doped layer was formed by N-type ion implantation with a dose of 5×10^{14} cm^{-2} and energy of 40 keV onto the top silicon layer. The heavy doping for ohmic contact on Si was formed by implanting a further dose of 4×10^{15} cm^{-2} of phosphorus ions at 20 keV on the basis of the injection in the PD N region, as shown in Fig. 2b. In order to activate the implanted phosphorus ions and repair the implantation damage, the rapid thermal annealing (RTA) was performed after the implantation at 1050 °C for 5 s.

At first, a SiO_2 layer with a thickness of 1 µm was deposited, and then thinned to 500 nm by a chemical mechanical polishing (CMP) technique while smoothing the wafer surface. Subsequently, an epitaxial window of 15 µm length, 500 nm depth, and widths of 1 µm, 2 µm, 3 µm, 4 µm, and 5 µm was etched in the SiO_2 layer. The Ge-layer was deposited in two-step growth method. In order to prevent the emergence of voids at the top perimeter of the epitaxial window, the high temperature germanium layer is usually grown thick enough to completely fill the epitaxial window. Therefore, after Ge epitaxial growth, CMP was used to remove the excess Ge and the wafer surface fulfill the requirement of surface smoothness for the subsequent lithography process. The P region of the PIN structure was completed by implanting boron ions with energy of 10 keV and a dose of 3×10^{15} cm^{-2} in a specific region of the Ge layer. The width of the ion implantation region is usually smaller than the width of Ge-layer to reduce the electric field strength of the germanium layer and the dark current [8]. Finally, an annealing treatment at 600 °C for 60 s was applied to activate the boron ions implanted in the Ge and to avoid any severe re-diffusion of phosphorus ions during the thermal annealing.

In order to reduce the contact resistance, a layer of nickel is deposited on the bottom of the contact hole of germanium and silicon by physical vapor deposition (PVD) technology, followed by annealing at 500 °C for 30 s in an RTA chamber to form nickel silicon and nickel–germanium alloys. Finally, a standard CMOS process is used to form tungsten plugs, aluminum–copper electrodes, and SiO_2 passivation layers (not shown in Fig. 2).

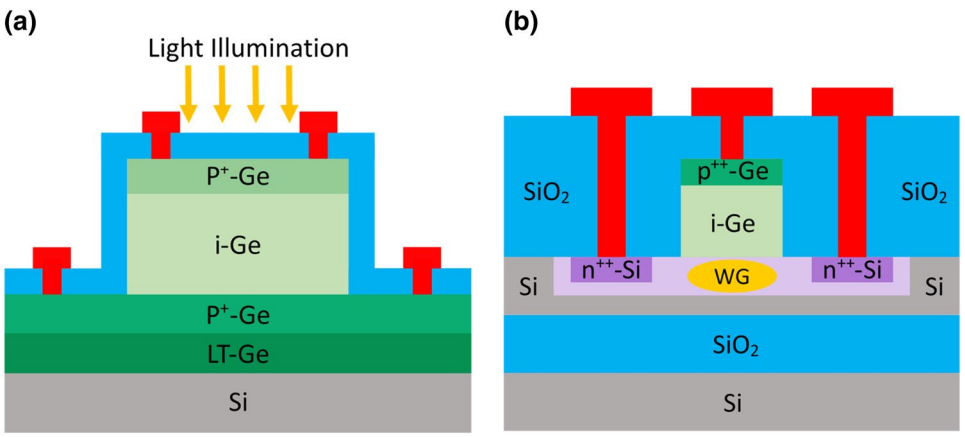


Fig. 2 Cross-section schematic of PIN Ge PDs structure deposited by **a** NSEG and **b** SEG and integrated with waveguide

3 Results and discussion

3.1 Methods to improve epitaxial quality of PIN structure

In this study, several methods have been examined to decrease the defect density in Ge layers which is the key issue for high performance detectors (see Fig. 3). One way to decrease defect density in Ge layer is to avoid a direct nucleation of Ge on Si surface by grading SiGe layer from Si to pure Ge. Figure 3a illustrates the cross-section TEM micrograph of the sample with graded-SiGe&HT-Ge structure. Since the thickness of the graded SiGe was only 300 nm, the Ge layer was not fully relaxed. Therefore, when the SiGe growth progresses and the epitaxial thickness increases, the accumulated strain energy is gradually released by the appearance of misfit dislocations in the graded SiGe. In order to decrease the defect density, the thickness of the graded SiGe layer should be considerably thicker (1 µm for 10% Ge-grading). Figure 3b illustrates LT&HT growth of Ge layer. In spite of some threading dislocations, most of the dislocations were buried in the low-temperature Ge buffer layer. This shows that the crystal defects due to the lattice mismatch between Si and Ge can be sufficiently suppressed by the present two-step growth process. It is important to notify that the quality of HT Ge layer improves by increasing the HT-layer thickness (usually above 1 µm the dislocation density is reduced to a level of 10^6 cm^{-2}) and further improvements occurs with an optimized post-annealing treatment.

Moreover, the impact of intrinsic layer thickness in PIN structure and post annealing on TDD has been studied and the results are summarized as shown in Table 1. We would like to emphasize that the NSEG detectors have two groups in Table 1. The first group (NSEG1) has no post-annealing treatment meanwhile the rest of the detectors (NSEG2) have been annealed at 820 °C for 20 min in H_2 to reach the defect TDD in level of 10^6 cm^{-2}.

For NSEG1 detectors, the thickness of the intrinsic layer was varied from 300, 700 to 1000 nm. The layer

Table 1 Dark currents for Ge photodetectors with different designs

	Intrinsic layer thickness (nm)	Area (µm^2)	Dark current (A)
NSEG (l)	300	2500	1.11E−05
	700	2500	8.44E−06
	1000	2500	5.55E−06
	1000	2500	5.55E−06
	1000	10,000	1.llE−05
	1000	22,500	3.70E−05
	1000	40,000	6.21E−05
	1000	62,500	1.17E−04
NSEG (2)	1000	79	4.30E−09
	1000	314	1.31E−08
	1000	1257	5.19E−08
	1000	2827	1.06E−07
	1000	5027	1.67E−07
	1000	7854	2.91E−07
SEG	500	15	7.32E−09
	500	30	2.21E−08
	500	45	3.66E−08
	500	60	4.23E−08
	500	75	7.10E−08

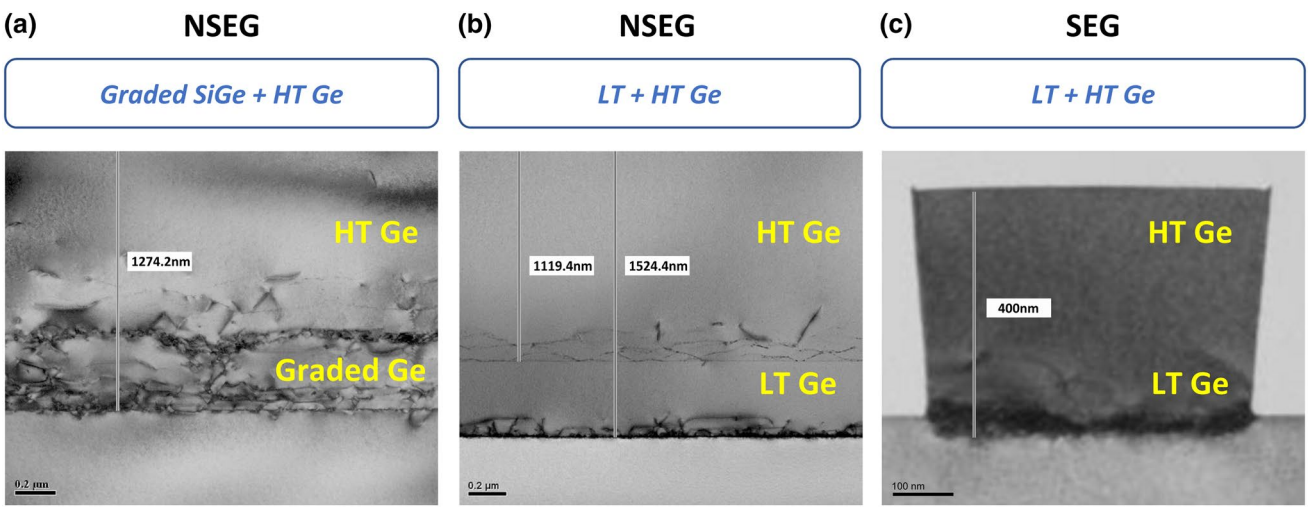


Fig. 3 Cross-section TEM images of the **a** graded SiGe grown on Si substrate, **b** two-step Ge grown on Si substrate, **c** two-step Ge grown on patterned SOI substrate using selective epitaxial growth

quality improves for thicker intrinsic layers and the dark current decreases following the layer quality improvement. The thickness variation of the intrinsic part (300, 700 and 1000 nm) in these samples results in defect density 10^{10} cm^{-2}, 10^{8} cm^{-2} and 10^{7} cm^{-2} where the measured dark current were 11.1 µA, 8.4 µA and 5.6 µA, respectively. In these detectors, there are almost a linear dependency between the dark current and TDD values. Therefore, this behavior shows that carrier generation-recombination process occurring at the defect centers is probably dominated in performance of detectors.

Previous studies have shown that optimization of passivation on the Ge surface can also improve dark current characteristics of the detector [13, 14]. The NSEG detectors prepared in this study did not include any special surface passivation on Ge, and its overlying TEOS SiO_2 as its passivation layer, and the surface states introduced by a large number of dangling bonds on the Ge surface after CMP increase the dark current of the detector [15].

3.2 Impact of epitaxy method on detector performance

There is a general view in epitaxy of semiconductors that SEG has a superiority to NSEG in terms of lower defect density. This relates to the reason that the growth occurs inside of trenches in SiO_2 layer and the dislocations may be terminated to the oxide walls resulting lower defect density. Figure 3c illustrates a high epitaxial quality of Ge layer deposited on the Si waveguide. At this stage, the dark current of both Ge NSEG and SEG PDs were characterized as shown in Fig. 4a and b. The level of dark current is almost the same in the figures meanwhile it decreases by decreasing the area of detectors. More detailed analysis shows that dark current density verses area is almost unchanged for both SEG and NSEG detectors.

This is obvious from Fig. 4 that the dark current increases by increasing the reverse bias. The best dark current values from the non-selectively and selectively grown PDs were 4 nA (for D = 10 µm) and 7 nA (Ge width 1 µm and length 15 µm) at − 1 V, respectively. These values show the dark current of SEG PDs is slightly higher than NSEG PDs although the thickness of the intrinsic layer for SEG PDs was only 500 nm. This indicates that the epitaxial quality of SEG Ge layer is a significant issue and it could be better than in NSEG layers.

Figure 5a, b illustrate the behavior of both dark current and the photo current. Both dark current and photocurrent increase with increasing detector area. The increase of photocurrent is due to the absorption of more photons in the larger area meanwhile the decrease of dark current could be due to less contact resistance and defects in smaller detector areas.

In the process of SEG samples, it is important that the trench oxides will not be formed by a single one-step dry etching due to the damage of the bottom silicon surface caused by the over-etching. Using a combination of dry and wet etching to create an epitaxial window is necessary for the high quality epitaxial Ge.

3.3 Responsivity of NSEG and SEG Ge detectors

Another important parameter for the detector performance is responsivity (R). This parameter is defined as following:

$$R = I_{ph}/P_o = \eta q\lambda/hc \quad (1)$$

where I_{ph} is the photocurrent, P_o is the optical power incident on the PD, η is the quantum efficiency, q is the electrical charge, h is Planck's constant, c is the speed of light. For

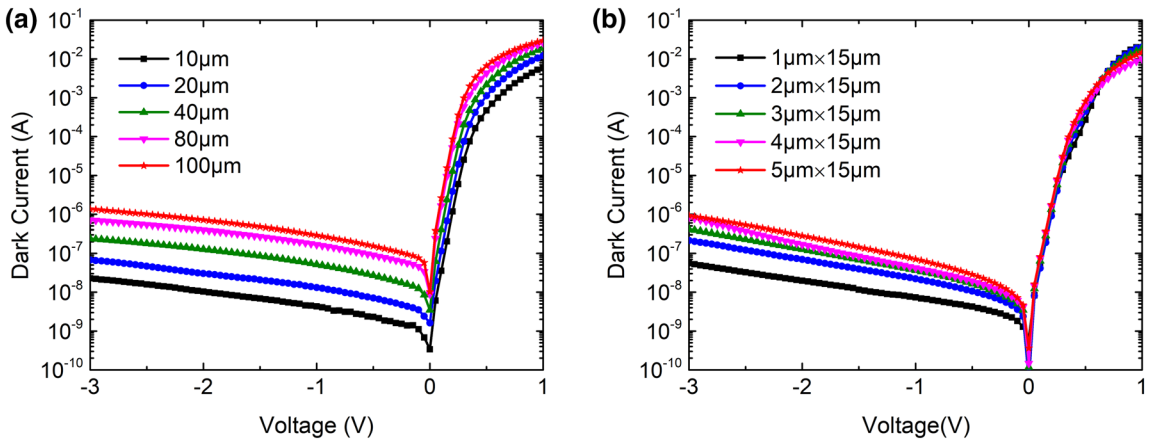


Fig. 4 Dark current of PDs with different areas **a** NSEG detectors with diameters of 10, 20, 40, 80, and 100 µm and **b** SEG filled trenches 15 µm long and: 1, 2, 3, 4, and 5 µm wide

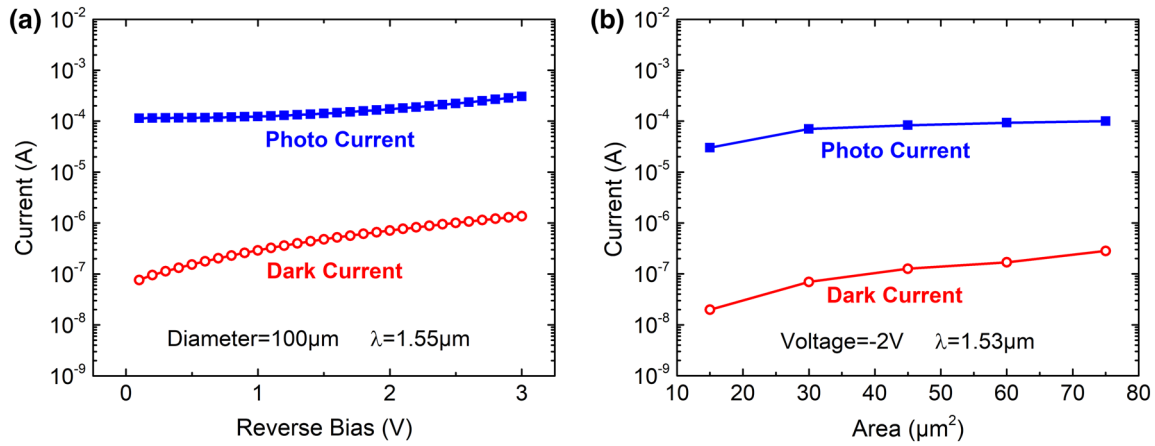


Fig. 5 **a** Current–voltage characteristic of the 100-μm-diameter device under illumination of 1550 nm light and **b** current–area characteristic of the device under the illumination of 1530 nm light

such measurements, a tunable laser is required for the I–V test system. The optical power entering the NSEG detectors was 1 mW and it was ~ 1.07 mW during the test of SEG detectors. After deducting the loss of the entire optical link (mainly including the coupling loss of the grating, the transmission loss of the waveguide, and the end surface reflection loss of the fiber joint), the actual optical power entering the SEG detector is ~ 0.215 mW.

Figure 6a, b show the responsivity of NSEG and SEG PDs versus the bias voltage and detector area, respectively. The measured values are in range of the responsivity values of Si-based Ge PDs reported by various research groups (0.4–0.8 A/W) [16–18]. In Fig. 6a, the responsivity of NSEG detectors increases by increasing the bias voltage (for example, for 1 to 3 V reverse bias, responsivity is 0.12–0.3 A/W). The increase of responsivity due to the increase of reverse voltage is easily conceivable from Eq. (1) since the photocurrent increases at higher reverse voltages. In fact, typical bias voltages should be in range of 1–2 V due to operating compatibility to CMOS circuits.

In Fig. 6b, the responsivity increases with increasing detector area for SEG PDs. Most of NSEG PDs show responsivity values in range of 0.05–0.12 A/W (not shown in the figure) which is remarkably lower responsivity than SEG PDs. In general, a low optical power enters into SEG PDs since the light propagates through waveguide (with energy loss) and is not shined by direct illumination. The reason for high responsivity is a compatible photocurrent is generated in SEG PDs compared to NSEG PDs.

Since the dark current becomes smaller for smaller detector areas (according to Fig. 5), therefore, it is important to choose a trade-off for detector area size to have a balance for low dark current and high responsivity [19].

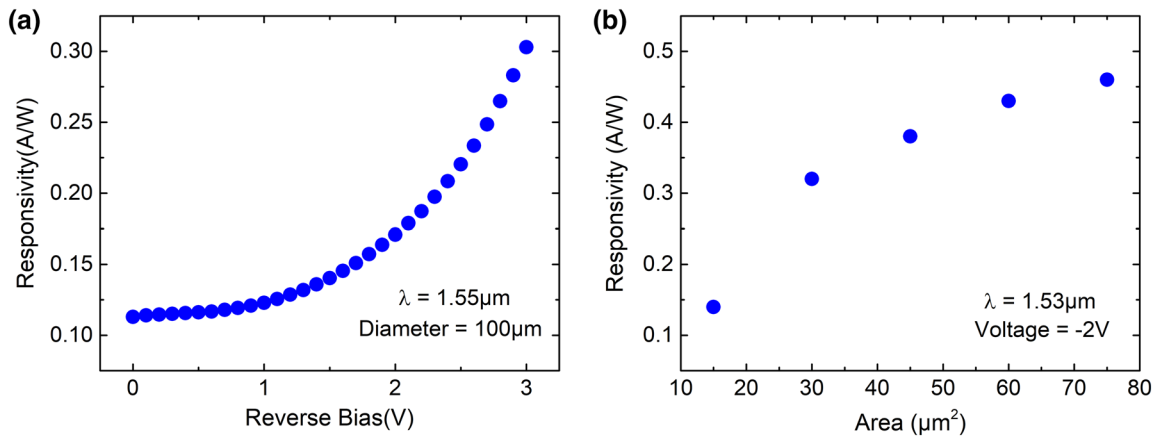
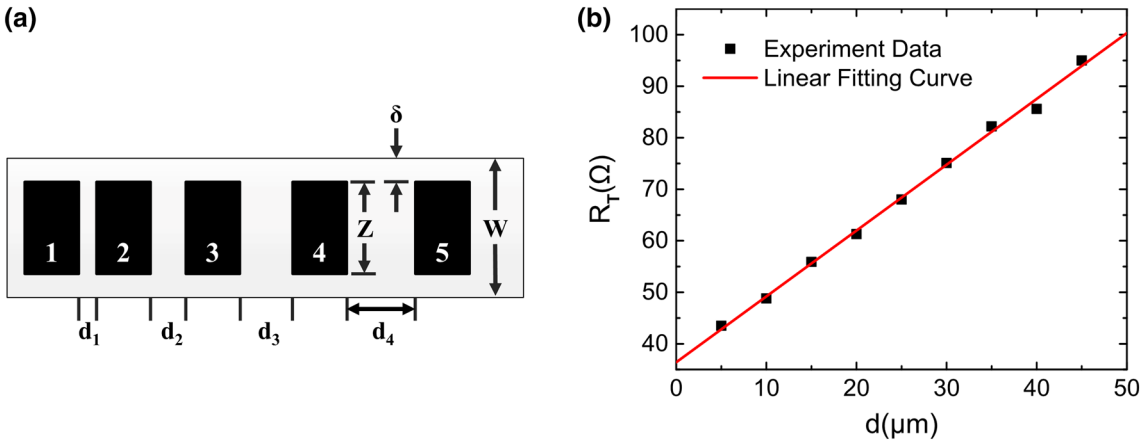


Fig. 6 **a** Responsivity versus reverse bias for the NSEG Ge PIN detector with a diameter of 100 μm, and **b** responsivity versus area for the SEG Ge PIN detector under the voltage of − 2 V



Fitted curve	$R_{sh}(\Omega)$	$L_T(\mu m)$	$R_C(\Omega)$	$\rho_c(\Omega \cdot cm^2)$
R_T=1.28d+36.5	128	14.3	18.3	2.6×10^{-4}

Fig. 7 **a** Chip layout of TIM mask, **b** resistance versus the pad distances

3.4 Contact resistance analysis

One of the most critical issues for performance of PD is the quality of the ohmic contact and the contact resistance. In this study we lowered the contact resistance by forming nickel-germanide on N-doped Ge in the PIN PD structure. To investigate the contact resistance separately from PDs we fabricated a TLM mask containing contact pads with different distances from each other (marked d_i). In the mask layout, the d_i values ranged from 5 to 45 μm at regular intervals of 5 μm, and the gap δ was 0.5 μm as shown in Fig. 7a. The total resistance (R_T) and contact resistivity (ρ_C) are calculated from the following formulas:

$$R_T = R_{sh} d_i / Z + 2R_C \tag{2}$$

$$\rho_C = (R_C^2 \cdot W^2)/R_{sh} \tag{3}$$

where Z is the width of the metal semiconductor contact, and W is the width of the entire semiconductor mesa. In above equation, R_{sh} stands for the square resistance of the semiconductor and R_C is contact resistance which can be obtained from the vertical intercept [20].

These measurements reveal a resistivity value of 2.6×10^{-4} Ω cm^2 as fitted in Fig. 7b. This value is not as low as for the p-doped Ge (in range of 10^{-6} Ω cm^2). The reason behind such behavior could be the damages during the implantation. Further study will be carried out to investigate and decrease the contact resistance to n-type doped Ge.

4 Conclusions

The performance of Ge PIN photodetectors with both selective and non-selective growth was evaluated. The epitaxial quality of Ge is the key issue and it relates to how effectively the starting LT-Ge grown layer has sealed the defects due to initial nucleation of Ge islands. Applying a SiGe as starting layer does not seem to be a good solution since a very thick layer has to be grown in order to hinder the defects from propagating to the HT-Ge layer. The contact resistance to n-type doped Ge is observed to be high and it acts as a source for the dark current and low responsivity.

Acknowledgements This work was financially supported by the National Key Research and Development Program of China (2016YFA0301701), and the Youth Innovation Promotion Association of CAS under Grant Nos. 2015097 and 2016112, which are acknowledged.

References

1. S. Luryi, A. Kastalsky, J.C. Bean, New infrared detector on a silicon chip. IEEE Trans. Electron. Dev. **31**, 1135–1139 (1984)
2. M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, E.A. Fitzgerald, Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing. Appl. Phys. Lett. **72**, 1718–1720 (1998)

3. S.B. Samavedam, M.T. Currie, T.A. Langdo, E.A. Fitzgerald, High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers. Appl. Phys. Lett. **73**, 2125–2127 (1998)
4. Z. Huang, J. Oh, J.C. Campbell, Back-side-illuminated high-speed Ge photodetector fabricated on Si substrate using thin SiGe buffer layers. Appl. Phys. Lett. **85**, 3286–3288 (2004)
5. L. Colace et al., Ge/Si (001) photodetector for near infrared light. Solid State Phenom. **54**, 55–58 (1997)
6. S. Dongwoo, K. Sanghoon, J. Jiho, K. Gyungock, 36-GHz high-responsivity Ge photodetectors grown by RPCVD. IEEE Photonics Technol. Lett. **21**, 672–674 (2009)
7. Y. Hyun-Yong et al., High-efficiency p-i-n Photodetectors on selective-area-grown Ge for monolithic integration. IEEE Electron. Device Lett. **30**, 1161–1163 (2009)
8. T. Yin et al., 31 GHz Ge n-i-p waveguide photodetectors on Silicon-on-Insulator substrate. Opt. Express **15**, 13965–13971 (2007)
9. S. Lischke et al., High bandwidth, high responsivity waveguide-coupled germanium p-i-n photodiode. Opt. Express **23**, 27213–27220 (2015)
10. H. Chen et al., − 1 V bias 67 GHz bandwidth Si-contacted germanium waveguide p-i-n photodetector for optical links at 56 Gbps and beyond. Opt. Express **24**, 4622–4631 (2016)
11. H.H. Radamson, M. Kolahdouz, S. Shayestehaminzadeh, A.A. Farniya, S. Wissmar, Carbon-doped single-crystalline SiGe/Si thermistor with high temperature coefficient of resistance and low noise level. Appl. Phys. Lett. **97**, 223507–223507 (2010)
12. S.G.E. Wissmar, H.H. Radamsson, Y. Yamamoto, B. Tillack, C. Vieider, J.Y. Andersson, SiGe quantum well thermistor materials. Thin Solid Films **517**, 337–339 (2008)
13. J. Kang, R. Zhang, M. Takenaka, S. Takagi, Suppression of dark current in GeOx-passivated germanium metal-semiconductor-metal photodetector by plasma post-oxidation. Opt. Express **23**, 16967–16976 (2015)
14. M. Takenaka, K. Morii, M. Sugiyama, Y. Nakano, S. Takagi, Dark current reduction of Ge photodetector by GeO2 surface passivation and gas-phase doping. Opt. Express **20**, 8718–8725 (2012)
15. J.R. Weber, A. Janotti, P. Rinke, C.G. Van de Walle, Dangling-bond defects and hydrogen passivation in germanium. Appl. Phys. Lett. **91**, 142101–142101 (2007)
16. L. Colace et al., Efficient high-speed near-infrared Ge photodetectors integrated on Si substrates. Appl. Phys. Lett. **76**, 1231–1233 (2000)
17. Z. Zhou, J. He, R. Wang, C. Li, J. Yu, Normal incidence p–i–n Ge heterojunction photodiodes on Si substrate grown by ultrahigh vacuum chemical vapor deposition. Opt. Commun. **283**, 3404–3407 (2010)
18. Q. Fang et al., Demonstration of a vertical pin Ge-on-Si photodetector on a wet-etched Si recess. Opt. Express **21**, 23325–23330 (2013)
19. H.H. Radamson, L. Thylen, *Monolithic Nanoscale Photonics-Electronics Integration in Silicon and Other Group IV Elements*, (Elsevier, Amsterdam, 2014)
20. D.K. Schroder, *Semiconductor Material and Device Characterization*, (Wiley, New York, 2006)