

# A Comparison of Power Factor in *N* and *P*-Type SiGe Nanowires for Thermoelectric Applications

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This work presents the thermoelectric properties of *n*- and *p*-type doped SiGe nanowires and shows the potential to generate electricity from heat difference over nanowires. The Si<sub>0.74</sub>Ge<sub>0.26</sub> layers were grown by reduced pressure chemical vapor deposition technique on silicon on insulator and were condensed to the final Si<sub>0.53</sub>Ge<sub>0.47</sub> layer with thickness of 52 nm. The nanowires were formed by using sidewall transfer lithography (STL) technique at a targeted width of 60 nm. A high volume of NWs is produced per wafer in a time efficient manner and with high quality using this technique. The results demonstrate high Seebeck coefficient in both *n*- and *p*-types SiGe nanowires. *N*-type SiGe nanowires show significantly higher Seebeck coefficient and power factor compared to *p*-type SiGe nanowires near room temperature. These results are promising and the devised STL technique may pave the way to apply a Si compatible process for manufacturing SiGe-based TE modules for industrial applications.

**Keywords:** Thermoelectric, SiGe Nanowires, Power Factor, Sidewall Transfer Lithography, Condensation.

## 1. INTRODUCTION

The efficiency of SiGe as a thermoelectric (TE) material has been improved and the reported data indicate a peak of conversion efficiency at high temperature interval of 900–950 °C.<sup>1</sup> This is a reason that SiGe alloys have inaugurated a platform for satellites in space for conversion of radio-isotopic heat to electricity or other high temperature power generation applications. The efficiency of TE materials, ZT is considered as the dimensionless figure-of-merit and is expressed as

$$Z \times T = \frac{\sigma \times S^2}{\tau} \times T \quad (1)$$

where *S*, *σ* and *τ* are Seebeck coefficient, electrical conductivity and thermal conductivity, respectively. However, it is usually challenging to improve ZT because of strong interdependence of these transport coefficients. Recent developments on nanoscale materials have provided the possibility to further enhance the efficiency of

TE materials.<sup>2</sup> For example, nanowires (NWs) are one of the nanomaterial architectures which show capability to tailor the carrier transport and phonon conduction in a broad range of working temperatures.<sup>3–5</sup> This efficiency improvement is related to both reduction in thermal conductivity, because of surface and boundary scattering, and enhancement in power factor (*S*<sup>2</sup> × *σ*) due to manipulation of density of states around the Fermi level.<sup>3, 6–9</sup> For example, 50% enhancement in ZT was observed in nanostructured *p*-type SiGe compared to bulk SiGe and a ZT of 0.46 was reported for SiGe NWs, more than twice compared to radioisotope TE generator (RTG) samples used by NASA space flight due to only reduction in thermal conductivity.<sup>10, 11</sup>

Even though enhancement of the TE figure of merit (ZT) through reduction of thermal conductivity is vastly investigated, a complete optimization to obtain higher power factor is still missing. It was shown that *S*<sup>2</sup> × *σ* can be enhanced through quantum confinement and energy filtering effects. Hence a series of studies devoted a large effort to investigate the above concept on nanostructured TE materials.<sup>9, 12–14</sup>

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In this article, we report on the enhancement in power factor of both *n*- and *p*-type SiGe NWs with 60 nm width and 47% Ge content compared to previous reports so far.<sup>6,11</sup> This enhancement was attributed to electronic transport and structural quality of NWs. The NWs were processed through sidewall transfer lithography (STL) fabrication technique which is cost-effective and feasible for mass production. This paves the path to apply a Si compatible process for manufacturing TE modules for industrial applications.

## 2. EXPERIMENTAL DETAILS

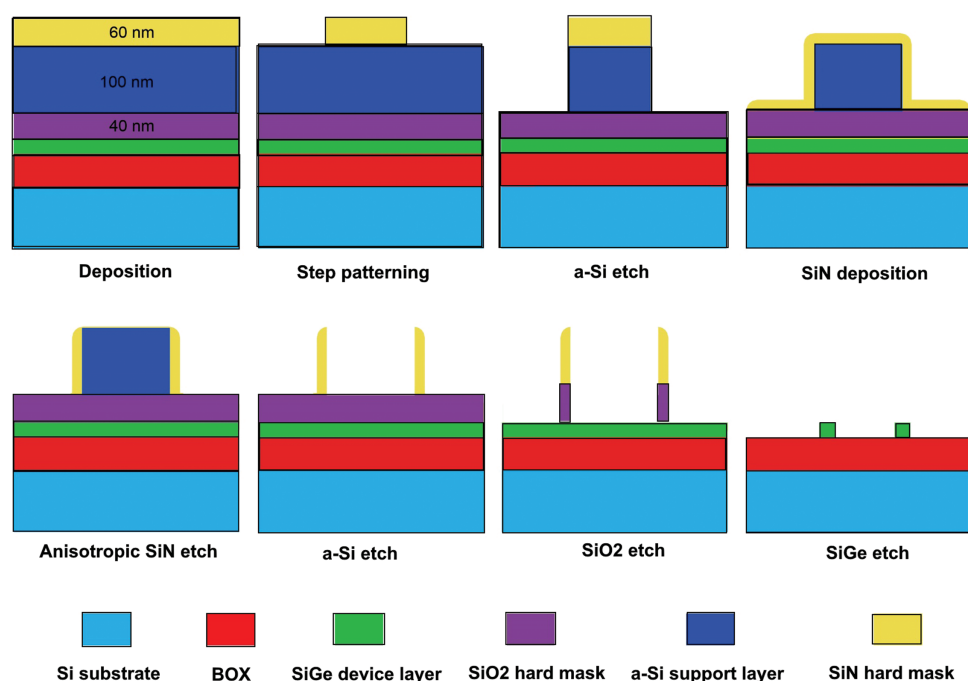
A stack of Si<sub>0.74</sub>Ge<sub>0.26</sub> (100 nm)/Si cap (10 nm) was epitaxially grown on Silicon on insulator (SOI) wafers with 50 nm Si top layer and 400 nm buried oxide. The wafers were loaded into the oxidation furnace for condensation of SiGe layer to higher Ge content. SiGe-on-insulator (SGOI) was manufactured by oxidation at 1050 °C for 90 min. The Ge content, layer thickness and the layer quality were determined by Rutherford back scattering technique (RBS) and high resolution X-ray rocking curves.<sup>15</sup>

The condensed SiGe layers were Boron (B) or Phosphorous (P)-doped by using diffusion method when B<sub>2</sub>H<sub>6</sub> or PH<sub>3</sub> was flown over the substrate at 700°C for 10 min in chemical vapor deposition (CVD) reactor. Four-probe measurement was used to determine the sheet resistivity.

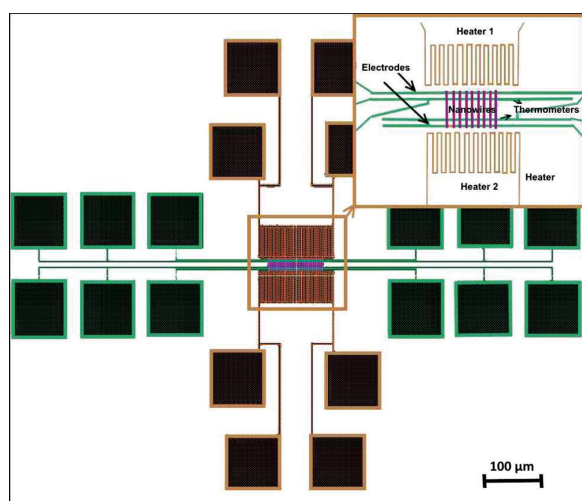
The doping concentration of *n*-type (P doped) and *p*-type (B doped) SiGe NWs was estimated as  $7 \times 10^{16}$  and  $10^{17}$  cm<sup>-3</sup> from sheet resistivity of 0.0854 and 0.0915 Ωcm, respectively. The higher incorporation of B in SiGe compared to P has been previously reported.<sup>16,17</sup>

In this step, STL technique was used to form NWs on *n*- and *p*-type SiGeOI wafers. Figure 1 displays the schematic view of the STL process. The width of NWs is defined with nitride spacer thickness, which is controlled by deposition time and conformal deposition of the material. The good control over the process in STL depends on control over the thickness of deposited materials and good selectivity of wet and dry etching and highly directional etching during the process.<sup>18,19</sup>

After the definition of NWs, metal electrodes thermometers and heaters were fabricated on both sides of NWs by evaporation of platinum (Pt) metal on patterned wafers. In order to assure ohmic contacts between nanowires and electrodes, 15 nm Nickel was deposited prior to the contact metallization followed by thermal annealing at 450 °C to form mono-crystalline of SiGeNi.<sup>20</sup> The temperature difference was obtained from the response of Pt thermometers resistivity when the heater is turned on applying DC current. The generated potential was measured using a Keithley 4200 SCS parameter analyser, which is used to calculate the Seebeck coefficient. The range of current and voltage measurement were 0.1 fA–1 A and 1 μV–210 V, respectively. For these measurements, the estimated noise of current and voltage were in interval of 10–100 pA and 10–20 μV, respectively. Two outer electrodes in the four probe configuration was used to measure electrical resistance of NWs, which is converted to electrical conductivity by using NWs dimensions. In order to confirm the generated TE potential over the NWs, the measurement was also performed by using the opposite heater. In this case, the values of voltage potential should be identical in magnitude but with opposite sign. The final structure



**Figure 1.** STL process steps to fabricate SiGe NWs.



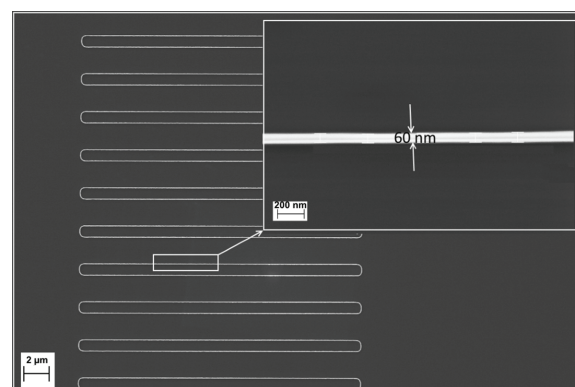
**Figure 2.** A schematic view of TE structure, inner electrodes act as thermometers and outer ones as electrical electrodes. Pt heaters are located on both sides of NWs.

of TE component used to measure NWs TE properties is displayed in Figure 2.

### 3. RESULTS AND DISCUSSION

Fabrication of NWs with high crystalline quality and regular shape is not an easy task. Different types of damages may occur during the processing step, which causes the electrical properties to be degraded. Most of the work on TE NWs is based on fabrication via bottom-up techniques and transfer of a single NW onto a prefabricated device.<sup>5, 11</sup> This method is quite impractical in terms of integration with other components in a chip or for mass production for industrial application. In this respect, top-down techniques can be considered as a good solution for semiconductor device fabrication. Electron beam lithography (EBL), ion beam lithography (IBL), scanning probe lithography (SPL) and focus ion beam (FIB) are some techniques which are trying to go beyond the limits of the optical lithography resolution for sub-100 nm NWs fabrication. The problems with most of these techniques are being not cost effective and time consuming. STL is one of the techniques which seems quite practical to overcome these issues in NWs fabrication.<sup>21, 22</sup> The SEM image of formed NWs using STL technique is shown in Figure 3. The SiGe NWs fabricated with STL are continuous and exhibit the targeted width of 60 nm. A high volume of NWs is produced per wafer in a time efficient manner and with high quality using this technique.

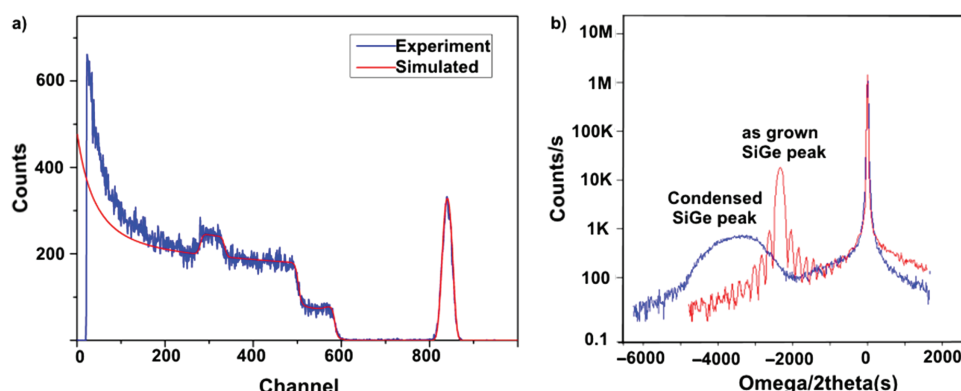
The Ge content and strain amount in the condensed SiGe layer are important issues since the electrical behavior of NWs depends on them. The mobility of SiGe is dependent on the bandgap and the strain amount and it increases with increasing Ge content.<sup>23, 24</sup> Figures 4(a and b) show the RBS result of condensed SiGe layer and rocking curves of SiGe layer before and



**Figure 3.** SEM image of SiGe NWs fabricated with STL technique.

after condensation. The simulated RBS result was used to estimate the Ge content as 47% and layer thickness of 52 nm, respectively. The broad shape of the condensed SiGe X-ray rocking curve with high full-width at half maximum (FWHM) value indicates a high defect density in the layer. The power factor, which is defined as  $S^2 \times \sigma$ , originates from electron density of states and electron effective mass.<sup>25</sup> In this case, the Seebeck coefficient becomes material dependent, and consequently the carrier mobility (or carrier scattering) will have a dominant effect as well. For TE materials a quite broad range of mobility and effective masses can be found. For example, SiGe with high mobility and low effective mass is well known as one of the excellent TE materials operational in high temperature application.<sup>1</sup> The power factor in SiGe mostly can be improved by tuning conductivity through either doping or Ge content, but not through enhancement of Seebeck coefficient. In case of SiGe NWs when resistance of NWs increases dramatically with reduction of NWs dimension, the role of the Seebeck coefficient will be more important to manipulate the power factor.

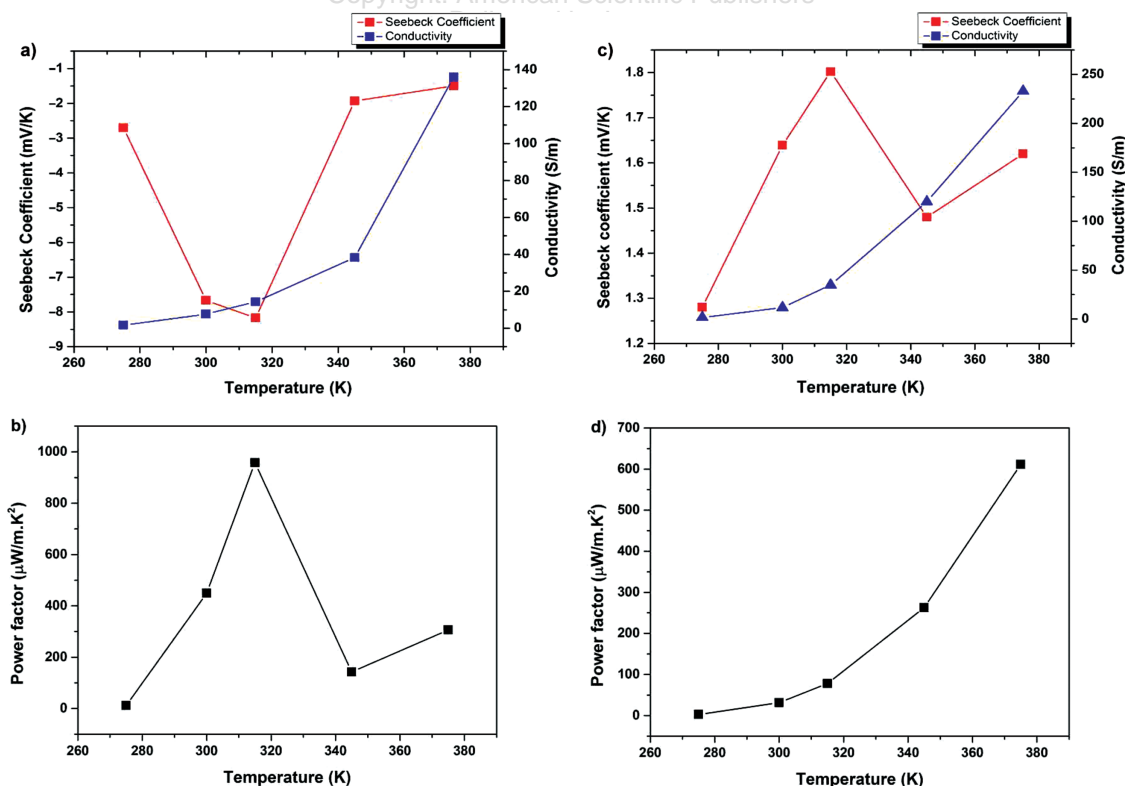
In this study, the Seebeck coefficient (as well as the power factor) of SiGe NWs is monitored by the dopant type. Figures 5(a and c) shows the Seebeck coefficient and electrical conductivity of lightly doped *n*-type and *p*-type SiGe NWs as a function of temperature. The value of the Seebeck coefficient generated by *n*-type SiGe has a maximum around 8 mV/K at 315 K, which even with low electrical conductivity obtained at this temperature can reach a power factor of 1000  $\mu\text{W}/\text{mK}^2$ . This value is remarkably higher than the published data for SiGe NWs so far (700  $\mu\text{W}/\text{mK}^2$  for  $\text{Si}_{0.63}\text{Ge}_{0.27}$ ).<sup>11</sup> This enhancement in power factor besides expectation for low thermal conductivity,<sup>11</sup> ensures high ZT for these types of *n*-type SiGe NWs. A Seebeck coefficient of 1.8 mV/K was observed for *p*-type SiGe NWs at similar temperature 315 K as shown in Figure 5(c). The high Seebeck coefficient can be obtained in lightly doped semiconductors when transport takes place away from Fermi level. Moreover the high Seebeck coefficient in both *n* and *p*-types SiGe NWs can be related to defects in layer, which were



**Figure 4.** (a) RBS spectrum of condensed SiGe layer and simulated one. (b) X-ray rocking curves of SiGe before and after the condensation.

created during condensation process. Both the experimental and theoretical work show that the significant enhancement of the Seebeck coefficient in semiconductors can be due to the sub-levels created within the bandgap which can act as potential barrier or energy filtering.<sup>12,13</sup> The mechanism behind energy filtering is based on subtraction of carriers with higher and lower energy level with respect to the Fermi level. Therefore, high energy carriers contribute to the Seebeck coefficient resulting in significant improvement in electrical characteristics.<sup>26</sup> On the other hand, it is known that the interaction of defects is temperature dependent. This could be the reason for the

appearance of a peak for *n*-type and *p*-type SiGe samples at 315 K. Further investigations are necessary to figure out the type of defects that are involved for the changes in the Seebeck coefficient. The maximum power factor of *n*-type  $\text{Si}_{0.53}\text{Ge}_{0.47}$  NWs is about two times higher than *p*-type  $\text{Si}_{0.53}\text{Ge}_{0.47}$  ones, as shown in Figures 5(b and d) respectively. Although the same diffusion process has been applied, the resistivity data shows that the dopant level of B for *p*-doped SiGe layer is higher than *n*-type ones. Therefore, the carrier mobility in *p*-type SiGe NWs is lower than *n*-type, which can cause the Seebeck coefficient in *p*-type SiGe NWs to be lower than *n*-type NWs.



**Figure 5.** Thermoelectric parameters: Seebeck coefficient-electrical conductivity and power factor of (a, b) *n*-type, and (c, d) *p*-type SiGe NWs. The error margin for the measured data is less than 5%.



#### 4. CONCLUSIONS

Low dimensional TE structures based on *p*- and *n*-type SiGe NWs with cross-section of 60 nm × 52 nm were fabricated using STL technique. The STL method is a Si compatible process using one-step lithography when a nitride spacer is formed as hard mask to define NWs. The maximum Seebeck coefficients were 8 mV/K and 1.8 mV/K for *n*- and *p*-type SiGe NWs at temperature 315 K, respectively which reveal excellent power factor values for SiGe material. This behavior of the power factor is attributed to potential barriers originating from the defects during condensation of SiGe and formation of NWs. This study shows promising results for the implementation of SiGe NWs in future TE generators.

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