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Unprecedented Thermoelectric Power Factor in SiGe Nanowires Field-Effect Transistors

Mohammad Noroozi,[a,b,z] **Ganesh Jayakumar,**[c] **Katayoun Zahmatkesh,**[a] **Jun Lu,**[b] **Lars Hultman,**[b] **Mounir Mensi,**[a] **Saulius Marcinkevicius,**[a] **Bejan Hamawandi,**[a] **Mohsen Y. Tafti,**[a] **Adem B. Ergül,**[a] **Zoran Ikonic,**[d] **Muhammet S. Toprak,**[a] **and Henry H. Radamson**[c,z]

[a]*Department of Applied Physics, KTH Royal Institute of Technology, SE 10691, Stockholm, Sweden*
[b]*Department of Physics, Chemistry and Biology (IFM), Linköping University, SE-581 83 Linköping, Sweden*
[c]*Department of Components and Circuits, KTH Royal Institute of Technology, SE 16440 Kista, Stockholm, Sweden*
[d]*Faculty of Engineering, University of Leeds, Leeds, UK*

In this work, a novel CMOS compatible process for Si-based materials has been presented to form SiGe nanowires (NWs) on SiGe On Insulator (SGOI) wafers with unprecedented thermoelectric (TE) power factor (PF). The TE properties of SiGe NWs were characterized in a back-gate configuration and a physical model was applied to explain the experimental data. The carrier transport in NWs was modified by biasing voltage to the gate at different temperatures. The PF of SiGe NWs was enhanced by a factor of >2 in comparison with bulk SiGe over the temperature range of 273 K to 450 K. This enhancement is mainly attributed to the energy filtering of carriers in SiGe NWs, which were introduced by imperfections and defects created during condensation process to form SiGe layer or in NWs during the processing of NWs.

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The search for high-performance thermoelectric (TE) materials for energy conversion applications has successfully progressed for more than four decades. Although tremendous achievements have been made, the discovery of materials and processes, which are cost effective and environmental friendly are still under intensive investigation. A fundamental new approach is needed to market this technology for mass production. In general, the TE efficiency is described via the dimensionless figure-of-merit (ZT), which is based on the electronic and phonon transport properties according to the following equation:

$$ZT = \frac{\sigma \times S^2}{\kappa} T \qquad [1]$$

where S is the Seebeck coefficient, T the absolute temperature, σ the electrical conductivity and κ the thermal conductivity, respectively. In Equation 1, the product of $S^2\sigma$ is referred to as the thermoelectric power factor (TEP). Engineering parameters of ZT (S, σ and κ) separately in bulk materials is a challenge since these parameters are strongly correlated to each other. A route to overcome this issue is via nano-structuring or nano-engineering, which allows the de-coupling of this correlation.[1,2]

Among the most promising TE materials, group IV alloys have attracted a strong research interest worldwide.[3–10] For example, Silicon-Germanium (SiGe) bulk materials have demonstrated high TE conversion efficiency in the temperature range of 800–1000°C.[11,12] The ZT of n- and p-type SiGe has been reported around 1.3 at 900°C and 0.95 at 800°C, respectively, which enables their integration for high temperature power generation or waste-heat recovery/harvesting applications.[11,12] However, this efficiency becomes remarkably low at medium (500 K-900 K) and low temperatures (up to 500 K).

For low temperature range, SiGe NWs have recently attracted attention due to their larger reduction of thermal conductivity observed both due to alloy and boundary scattering.[13] Despite low thermal conductivity values below 1.2 W/m.K for $Si_{0.73}Ge_{0.27}$ NWs at temperatures below 450 K, ZT is still limited to a maximum value of 0.46 for these NWs.[9] For other material systems, e.g., InAs NWs was shown that quantum confinement effect could modify the TEP at low temperatures T< 100 K.[14] In principle, it has been difficult to observe this quantum confinement phenomenon in 1D system since it requires NWs with diameter of 5–30 nm, which is costly to fabricate.[5,15] In another study, enhancement of TEP in InAs NWs was observed when NWs were non-uniform creating quantum-dot-like states.[16] But in both of these cases, TEP was measured at low temperatures since the carrier scattering degraded the prominent quantum effects at higher temperatures.

A series of publications have reported improvement of TEP when potential barriers have been introduced to the system. For example, Bahk et al.[17] reported an enhancement of almost 50% for TEP in PbTe material using carrier energy filtering presented by impurities or dispersed nanoparticles. They calculated the optimal cutoff energy level and reported this to be a few k_BT above the Fermi level (E_F). Soon after, they reported ZT value up to 3 in n- type Mg_2Si-Sn is possible if electrons with energy lower than 0.4 meV can effectively be filtered out from transport.[18]

The influence of defects on TEP has also been reported in Si NWs. The presence of dislocations and dislocation-loops showed significantly enhanced Seebeck coefficient to 1.81 mV/K for Si NWs with 750 nm diameter at room temperature. These defects act as potential barriers which, despite a decrease of mobility and electrical conductivity, lead to overall two-fold enhancement in TEP.[19]

This work presents a novel process to form SiGe NWs on oxide with high TE performance where the electrical and thermal transport could be affected by Ge content and defect density. Furthermore, the carrier transport was controlled by applying back-gate voltage and temperature affecting TE performance of NWs. In this way, The TEP of SiGe NWs was enhanced by a factor of >2 in comparison with SiGe bulk material over the temperature range form 273 K to 450 K. The electrical behavior of NWs was explained by potential barriers which were created due to the surface roughness of NWs, non-uniformity of composition of SiGe and the presence of defects in NWs.

Experimental

In this study, the process wafers were SIMOX with 340 nm Si and 400 nm buried oxide layer (BOX). The top Si layer was initially thinned down to 50 nm using dry oxidation at 1250°C. The formed oxide was stripped and the wafers were chemically cleaned prior to epitaxy of 100 nm $Si_{0.74}Ge_{0.26}$/10 nm Si cap. These wafers were loaded into the oxidation furnace at 1050°C for 90 minutes for condensation of SiGe layer to higher Ge content. During the oxidation, preferably Si atoms are mainly oxidized and the Ge will diffuse out. The buried oxide in the SOI wafer will act as diffusion barrier for Ge atoms during SiGe oxidation. The defect density in SGOI was reduced by post annealing at 850°C for 60 minutes in N_2. In this way, SiGe layers are condensed to high Ge content and any surface roughness which usually occurs in epitaxy of SiGe with high Ge content is not involved. Figure 1 demonstrates a schematic of the condensation process.

[z]E-mail: noroozi@kth.se; rad@kth.se

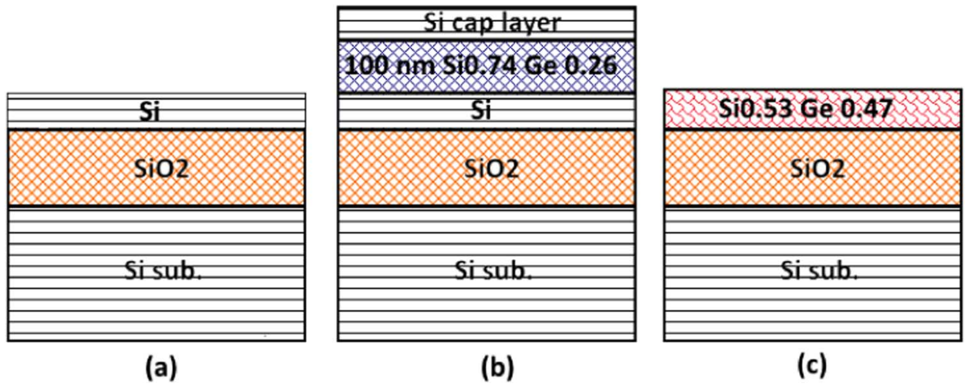

Figure 1. Schematic description of the condensation process; a) SOI wafer after thinning top Si to 50 nm b) Epitaxial growth of SiGe and Si cap layer, c) Single isolated SiGe layer from substrate after oxidation at 1050°C for 90 min followed by 850°C annealing for 60 minutes and stripping SiO_2 top layer.

The condensed SiGe layer was lightly Boron-doped by diffusion when B_2H_6 gas was blown over the substrate at 700°C for 10 min in hydrogen atmosphere in the chemical vapor deposition (CVD) chamber.

Hall measurement was performed to determine the carrier concentration and mobility in SiGe layer. The result shows the samples was p-type and had a concentration of 10^{17} cm^{-3} and mobility of 100 cm^2/vs at room temperature.

NWs with width of 60 nm were processed by using STL technique. The principles of STL are already described elsewhere,[20,21] which is based on transferring a pattern through creating trenches in oxide followed by deposition of a sacrificial layer and then etching the deposited layer. As a result, a residual of deposited layer is remained at the circumference of trench, which can be later used as a hard-mask to etch the SiGe layer in beneath. In this case, the width of NWs is determined by the width of the hard-mask layer. After the formation of NWs, in order to have low contact resistance a 10 nm Ni layer was deposited and the samples were subject to rapid thermal annealing at 450°C to form Ni-SiGe phase.[22] In the next step metal electrodes were fabricated across NWs by evaporation of Ti/Pt and employing lift-off process. The stack of metals together with Ni-SiGe layer ensure ohmic contact to the NWs which is a crucial point for the carrier transport through NWs.

Since the NWs are formed on SGOI wafers with 400 nm buried oxide a back-gate configuration is provided by applying biasing voltage to the substrate as the electrical configuration was shown in Figure 2. In this way, the transport of carriers through NWs could be adjusted and the conductance of NWs could be tuned within the temperature range of 273–450 K. The SiGe NWs were electrically characterized by using a set-up measurement which consisted of a Cascade 11000 shielded probe station equipped with temperature controlled chuck from −40°C to 300°C. The NWs had four contacts, which provide for a four-probe measurement where two inner electrodes (Th1, Th2) are used for supplying the current and the two outer ones (C1, C2) for measuring the voltage, as shown in Figures 2a and 2b. To measure the Seebeck coefficient, a temperature difference is established between

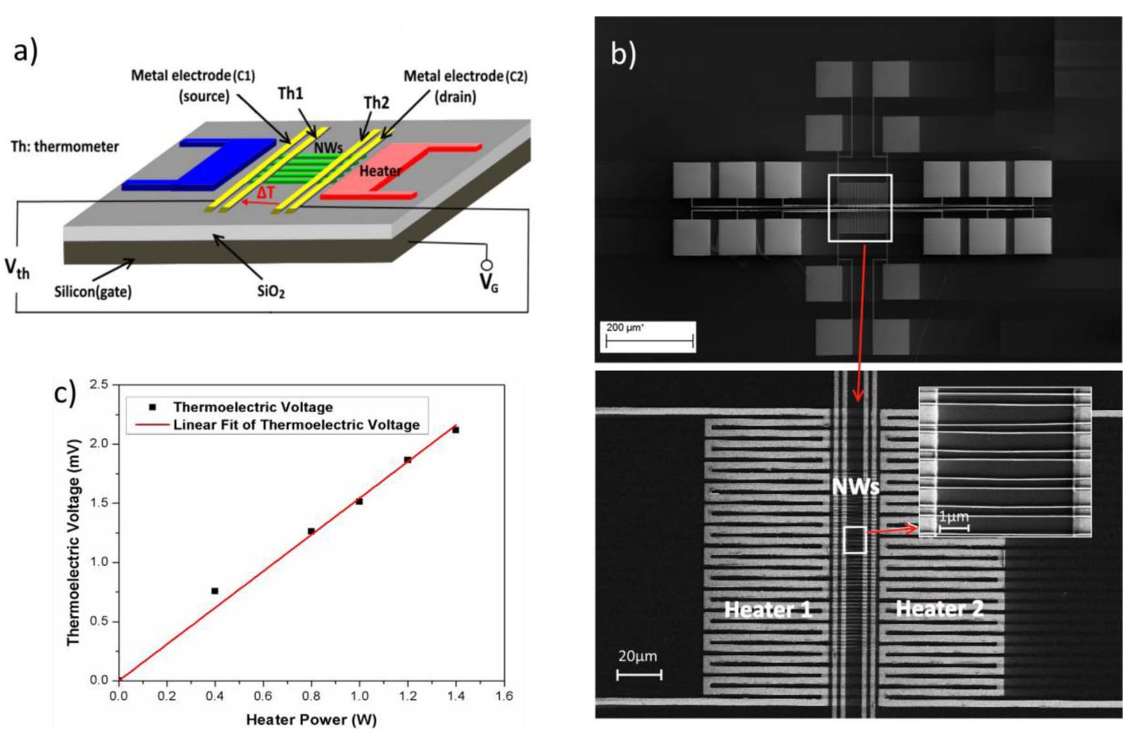

Figure 2. a) Schematic view b) SEM of the chip, where Th1 and Th2 acts as thermometer and for electrical measurement while C1 and C2 acts as electrodes to measure voltage difference c) Thermoelectric voltage versus heat power at 400K.

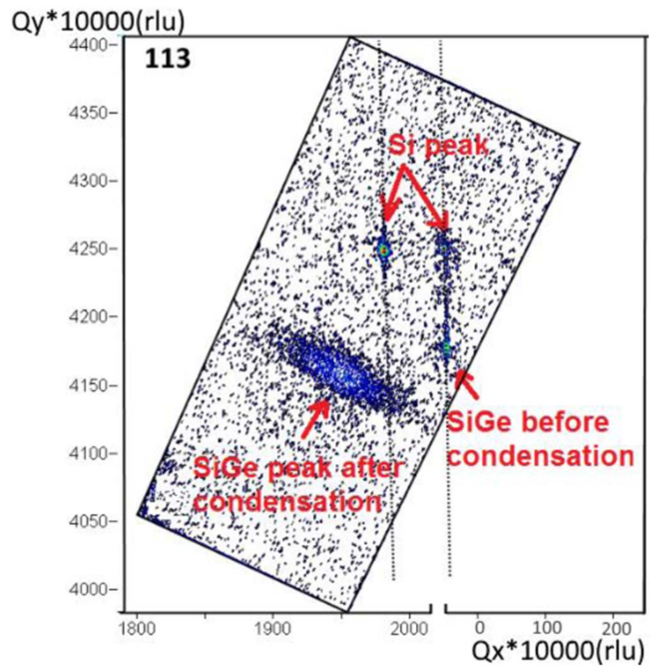

Figure 3. HRLLM of SiGe peak before and after condensation.

the two sides of NWs by the metal heater when a current is forced to heater contacts. The curve in Figure 2c shows how thermoelectric voltage generates with increasing heater power.

In this configuration, the inner electrodes (Th1, Th2) measure the resistivity, which is proportional to the temperature variation while the outer electrodes (C1, C2) measure the voltage drop across NWs. Moreover, the validity of temperature variation was evaluated using scanning probe microscope (Multiview 4000, Nanonics) equipped with a platinum-gold junction thermocouple probe (Nanonics) which scan along NWs. The resulting Scanning Thermal Micrograph, SThM, allows for the simultaneous measurement of the sample's morphology and local temperature with a submicron spatial resolution and an estimated relative temperature resolution of about 0.1 K.

The microstructures and defects were characterized by using an FEI Tecnai G2 TF 20 UT FEG microscope operated at 200 kV with 0.19 nm point resolution. The sample preparation was performed by a mechanically grounding of specimen to 50 μm thickness and subsequently ion thinning to electron transparency.

Results and Discussion

To interpret the TE performance of NWs the quality of SGOI samples was primarily investigated by high-resolution X-ray diffraction (HRXRD) to study the crystalline quality of SiGe layers. Figure 3 shows high resolution reciprocal lattice maps (HRRLMs) around (113) reflection from an as-grown Si/SiGe and the same sample after condensed by oxidation at 1150°C. Since the incident beam for (113) reflection is 2.8 degrees then a large area of the sample could be analyzed to detect defects.[23] The Ge content for as-grown and the condensed SiGe was 26% and 47% which were determined by the lattice mismatch parallel and perpendicular to growth direction obtained from the maps. These Ge contents were also confirmed by Rutherford back scattering (RBS) measurements. Since the wafers are SIMOX, there is no off-set or plane rotation in the Si/SiGe layers. Before the condensation process the Si and SiGe peaks are aligned along vertically with a series of interference fringes indicating strained SiGe layer with high quality interface. The thickness of SiGe layer is below the reported critical thickness for strain relaxation and the layer is totally strained. However, after condensation the SiGe peak is shifted further out from its position in the as-grown layer, and the shape is broadened along ω-direction (ω is X-ray incident beam). All these observations indicate that the defect density in the condensed SiGe is significantly larger than in the as-grown SiGe. Since no dislocations were observed in these samples, it is believed that the X-ray broadening feature is coming mostly from other types of defects. The strain relaxation in the condensed SiGe sample was estimated to be 90%.

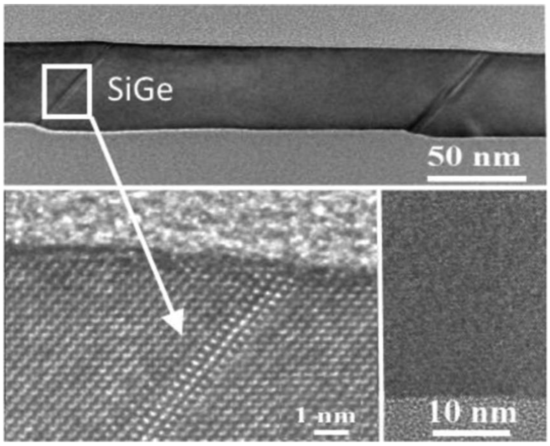

Figure 4. Cross section TEM image of condensed SiGe layer.

In order to estimate the defect density in the SGOI sample, high-resolution rocking curve in various reflections in the reciprocal space was performed and the evolution of the full width at half maximum (FWHM) of SiGe peak which is strongly correlated to the defect density was analyzed. Asymmetric (113), (224) and (115) reflections were measured and FWHM of three different reflections were used to model the defect density in SiGe layer using Equation 2 proposed by Ayers et al:[24]

$$D \sim \frac{\beta^2}{4.36 * b^2} \qquad [2]$$

where D stands for the defect density, β is the FWHM and b is the magnitude of Burgers vector. The values for the three asymmetric reflections were in reasonable statistical variation and showed SiGe layer contained defect density in the order of 10^{10} cm^{-2}.

Figure 4 shows cross sectional transmission electron microscopy (XTEM) micrograph of condensed SiGe layer. The TEM images show crystalline material with no dislocations or boron precipitations and defects are mainly stacking fault. This means that the SiGe layers are free of ionized centers and defects which could deform the surface of SiGe and disturb later the processing of NWs. The density of stacking faults in the SiGe layers was estimated to be in order of 10^8 cm^{-2}. This value is remarkably lower than the XRD measurements. One reason could be the presence of point defects which are difficult to be observed by TEM but easier to be detected by XRD.

In order to understand the thermal behavior of SiGe NWs the thermal maps were recorded for several heating power ranging from 0 mW to 1290 mW. In this way, the heat distribution over NWs and the surrounding can be observed and the temperature gradients are obtained for different heating powers. These values were used later to calculate the Seebeck coefficient along with measurement of generated voltage.

In such maps, a tip which is a thermocouple scans the surface and measures the temperature. Figure 5 shows the recorded temperature data for an area of the sample. The temperature gradient values are extracted for different input powers. For example, a temperature gradient of −0.12 K/μm was measured for the heating power of 1290 mW which implies a temperature difference of 0.84 K across the 7 μm length of the NWs between two inner electrodes. This value is in a perfect agreement with the result was extracted from resistor thermometer technique to measure temperature difference along NWs.

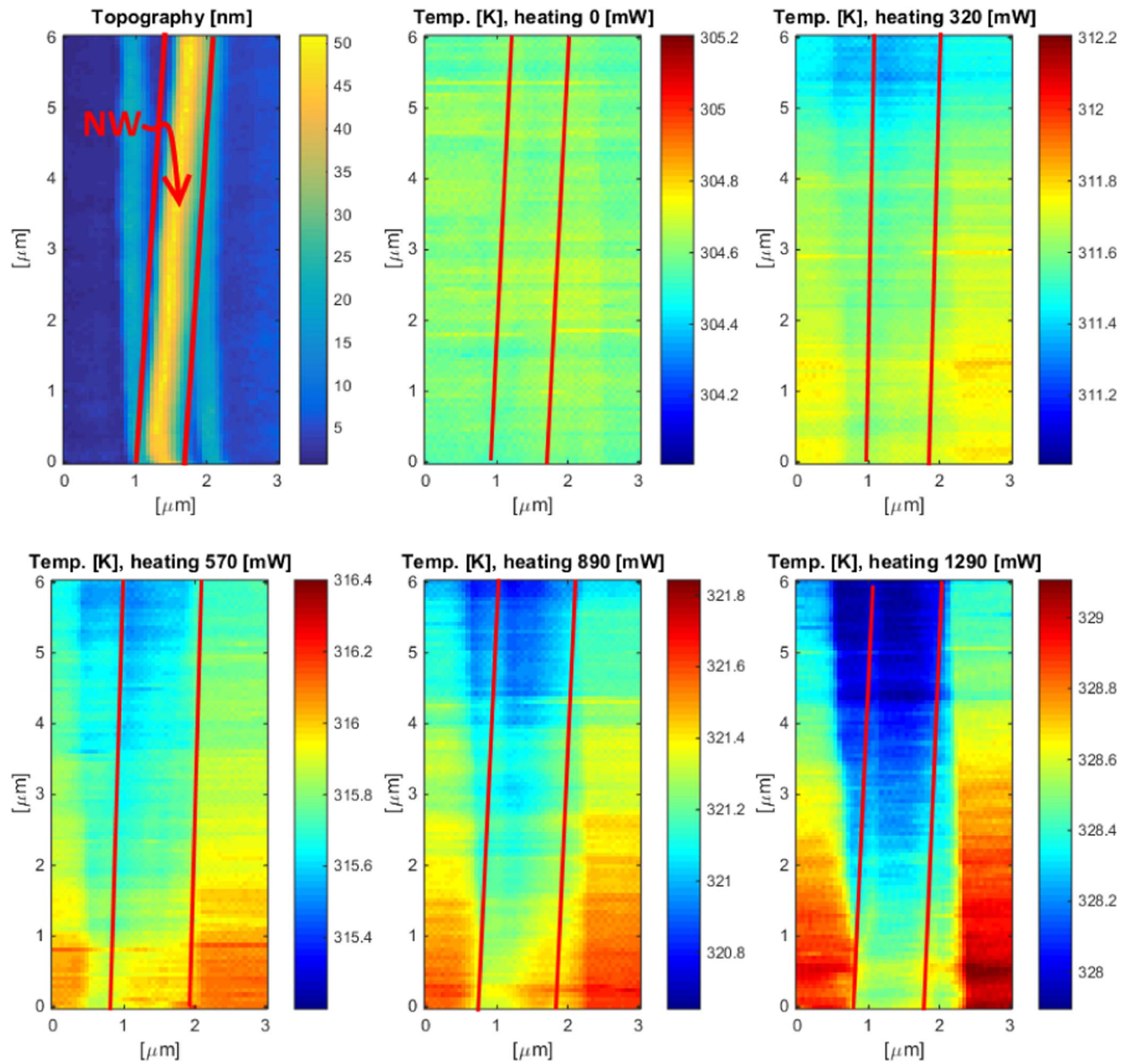

Figure 5. Topography (top left) and thermal maps of a single NW heated-up with heating power ranging from 0 to 1290 mW. The heating element is situated on the bottom of the maps. For clarity, the color range of the maps is kept constant.

The TE properties of SiGe NWs have been investigated using a back-gate configuration, which provides a bias voltage (V_G) in the range 0 to 20 V over the temperature range of 273 K to 450 K. The gate-biasing allows tailoring the electrical transport through NWs by changing the carrier density, i.e. the Fermi level position. For $V_G = 0$, the Seebeck coefficient of 2522 μV/K at 400 K was measured for the SiGe NWs. This value is almost three times higher than our theoretical calculation for the Seebeck coefficient of 790 μV/K for bulk SiGe at the same temperature and doping concentration. Figure 6 shows the measured TEP parameters for SiGe NWs, and the theoretically calculated parameters for SiGe bulk at 400 K is given for comparison. The theoretical calculations of the Seebeck coefficient, the electrical conductivity were made using the 8-band k.p method[25] which was considered for in comparison with experimental TE parameters of SiGe NWs. The electrical conductivity, displayed in Figure 6a, significantly increases with increasing the back- gate bias from 0.4 Ω/cm to 4.2 Ω/cm, with almost an order of magnitude improvement. In contrast, the applied bias voltage has only a modest influence on the Seebeck coefficient, which changes from 2522 μV/K to 2164 μV/K at 400 K.

Both the increase of electrical conductivity and decrease of Seebeck coefficient of NWs by increasing the back-gate bias were expected. By increasing the gate bias more carriers are arranged in the transport through NWs resulting the carrier concentration is increased. This interpretation is easily made according to Equations 3 and 4. The Seebeck coefficient, S for metals and degenerated semiconductors is given by:

$$S = \frac{8\,\pi^2 {K_B}^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}} \qquad [3]$$

where m^* stands for effective mass and n is the carrier concentration.[26] The electrical conductivity (σ) is related to n and the carrier mobility

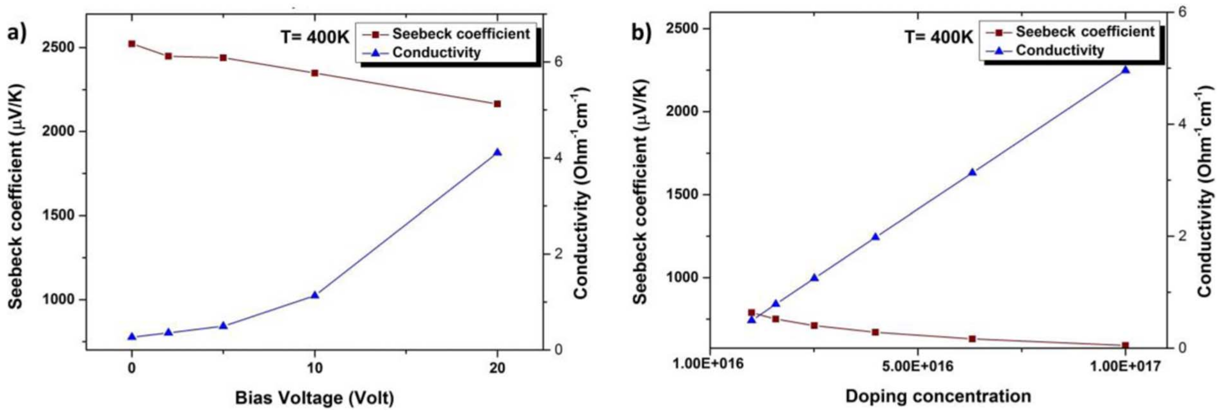

Figure 6. a) Experimentally measured transport coefficients in 60 nm wide SiGe NWs at 400 K, and (b) theoretically calculated values for bulk SiGe at the same temperature.

(μ) as follows:

$$\sigma = ne\mu \quad [4]$$

Since the semiconductor is lightly doped then the carrier mobility is high and by applying higher back gate voltage, n is increased however the dopant atoms which could act as scattering centers are missing.

The theoretical model in Figure 6b confirms also the above interpretations about electrical conductivity and Seebeck coefficient in SiGe material. To explain the behavior of the Seebeck coefficient, a detailed structure of SiGe NWs should be considered. It has been previously shown that filtering effect due to nanoscale potential barriers in the material can enhance the Seebeck coefficient and consequently the value of TEP.[27] In condensed SiGe layer the defects are generated due to strain relaxation of this layer, as shown in HRLLM map and TEM results. These defects constitute trap levels inside the bandgap and act as potential barriers for the charge carriers. These potential barriers can restrict movement of low energy carriers and allow only those with high energy to participate in transport. As a result, the average carrier energy is increased as well as the Seebeck coefficient when the electrical transport is through the high-energy carriers.

At this stage, the NWs chip was analyzed by HRTEM to ensure the defect density in SiGe has not changed during thermal treatments in processing step. Figure 7 demonstrates the top-view of NWs. Two points attract the attention for NWs in these micrographs. At first, the NWs have rough and wavy shape but they are crystalline. Secondly, there is a change in brightness along NWs which is diffraction contrast due to slight deviation of crystal orientation.

The composition variation was checked with energy dispersive X-ray (EDX) measurements tracing for Ge, Si and SiGe elements. These results indicate a slight compositional variation across the vertical diffusion direction during the condensation process in the SiGe layer. At this step, the behavior of the SiGe NWs was characterized in terms of the Seebeck coefficient and electrical conductivity for different V_G and temperatures. This allows an estimation of overall TEP ($S^2\sigma$) at different biasing over this range of temperatures. It can be seen from the electrical conductivity trend in Figure 8a that σ increases with

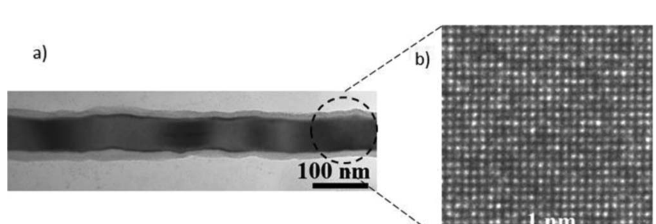

Figure 7. TEM images of a NW in a) low magnification and b) high resolution of a selected area in the NW.

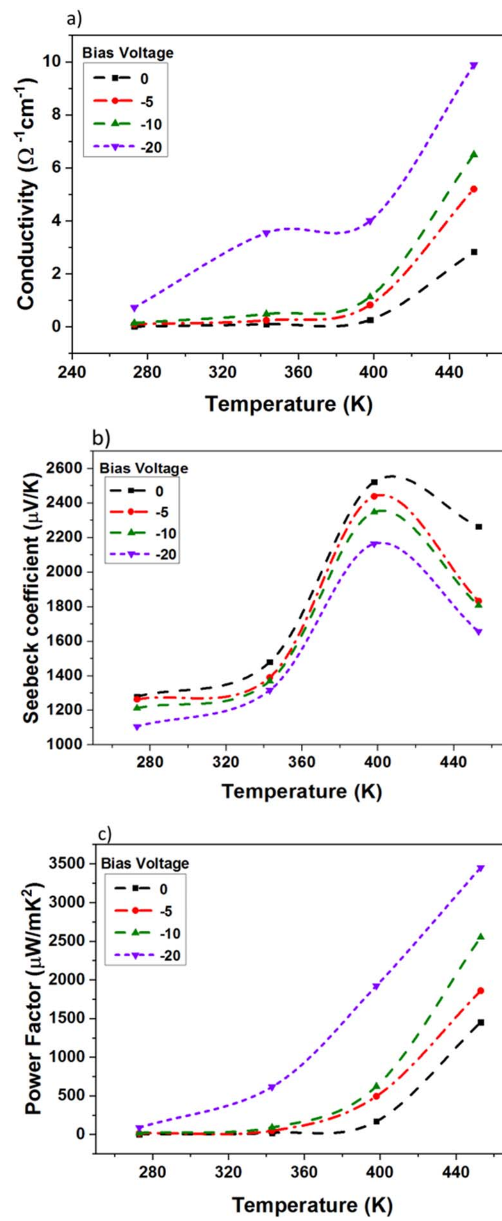

Figure 8. Thermoelectric parameters of 60 nm $Si_{0.53}Ge_{0.47}$ NWs as a function of temperature from 3 different samples with error of 5%: a) electrical conductivity, b) Seebeck coefficient, c) power factor (TEP).

increasing temperature. This behavior is expected in semiconductors when the bandgap shrinks and the intrinsic carrier concentration is increased with increasing temperature. Figure 8b demonstrates the dependency of the Seebeck coefficient on the temperature. The curve shows an initial decline but then increases to a peak value of 2522 μV/K at 400 K. The slight decrease of the Seebeck coefficient occurs for all temperatures, which demonstrates that although the Fermi level, measured from the band edge, increases with increasing V_G, the barrier height (optimum cut off energy level) remains few k_BT and consequently the Seebeck coefficient remains almost unaffected. Therefore, the TEP values in Figure 8c consistently follow this trend with temperature, due to both a high Seebeck coefficient and a large enhancement of electrical conductivity. In this study, the TEP values of SiGe NWs are considerably high in comparison with our theoretical calculation for bulk SiGe and also earlier reports[9,28,29] on SiGe NWs. For example, at 450 K and at $V_G = 20$ V the TEP exceeds the best possible theoretical calculated TEP value in bulk SiGe at the optimum doping concentration of 10^{19}, with a 2–fold enhancement.

In summary, SiGe NWs with a width of 60 nm were processed on SGOI wafers by using STL technique. The carrier transport in NWs was modified by the applied voltage to the gate at different temperatures. The first observation of remarkable enhancement of the Seebeck coefficient for SiGe NWs was reported in this study, assisted by defects, non-uniformity of SiGe and the roughness of NWs' shape. The defects and non-uniformity of SiGe are related to condensation process of SiGe layer meanwhile the roughness of NWs' shape is controlled during fabrication of NWs by STL technique. According to our measurements, a 2- fold enhancement of TEP was achieved for SiGe NWs, compared to bulk SiGe at similar temperatures. The results presented in this study demonstrate the advantages and high potential of material process and the fabrication technique for future mass production of TE modules for industry related applications.

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Authors MN wrote the main manuscript text and performed main part of fabrication and characterization, GJ contributed to the fabrication of nanowires, BH contributed to condensation process, KZ perform electrical characterization, LH and JL perform TEM characterization, MYT reviewed the manuscript and MM and SM performed thermal analysis, ZI performed theoretical calculation, ABE, MST and HHR reviewed and finalized the manuscript and All authors reviewed the manuscript. The authors declare no competing financial interests.

ORCID

Mohammad Noroozi http://orcid.org/0000-0002-4034-6415

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